FIG. 1

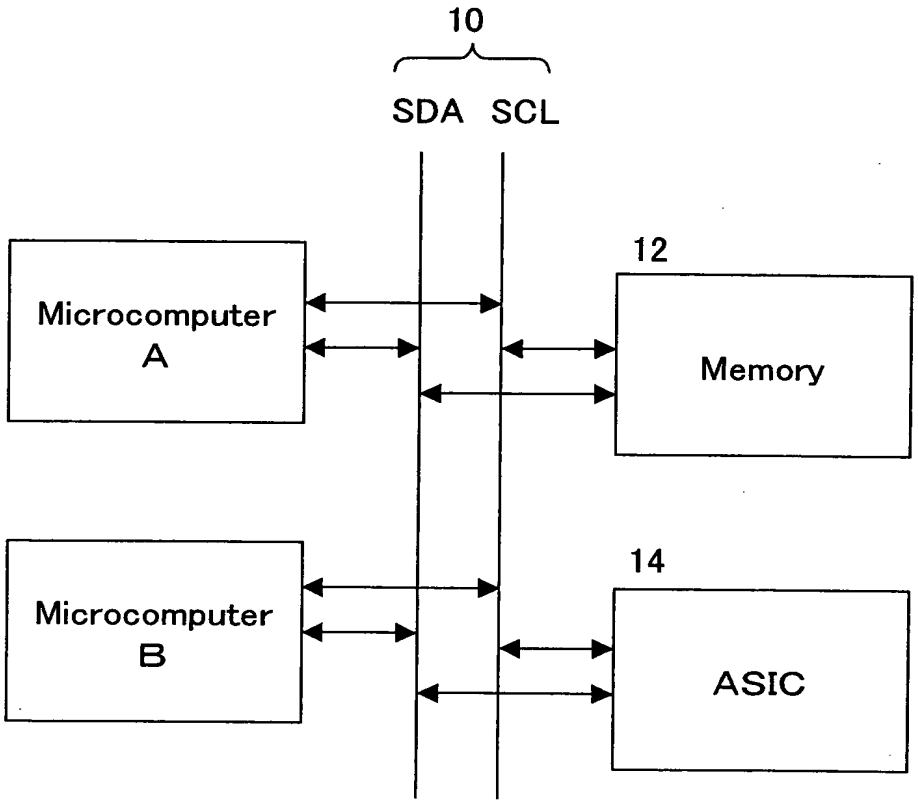

10
SDA
SCL
12
Microcomputer A
Memory
14
Microcomputer B
ASIC

FIG. 2

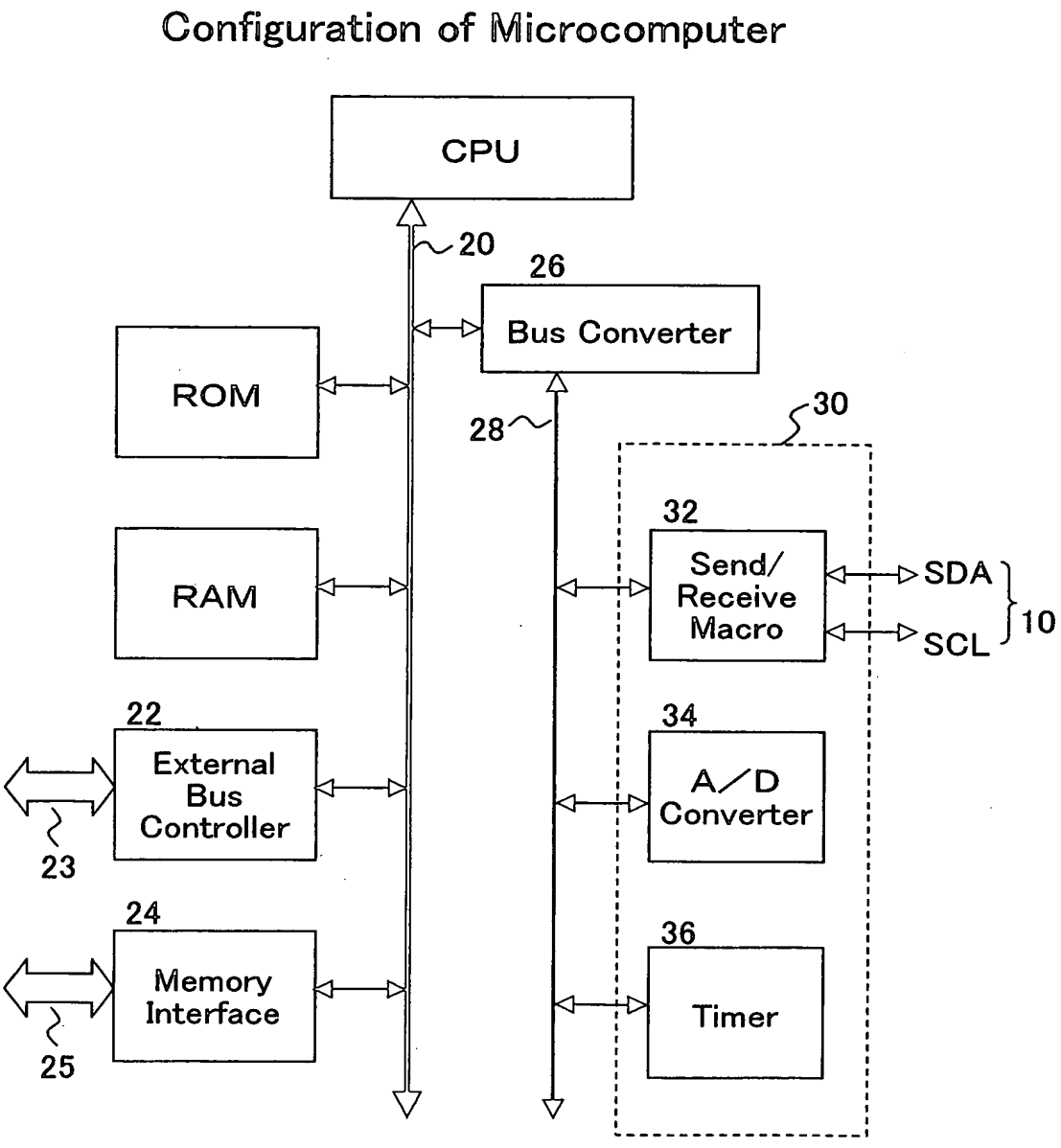

Configuration of Microcomputer
CPU
20
26
Bus Converter
ROM
28
30
32
RAM
Send/
Receive
Macro
SDA
SCL
10
22
External
Bus
Controller
34
A/D
Converter
23
24
Memory
Interface
36
Timer
25

FIG. 3

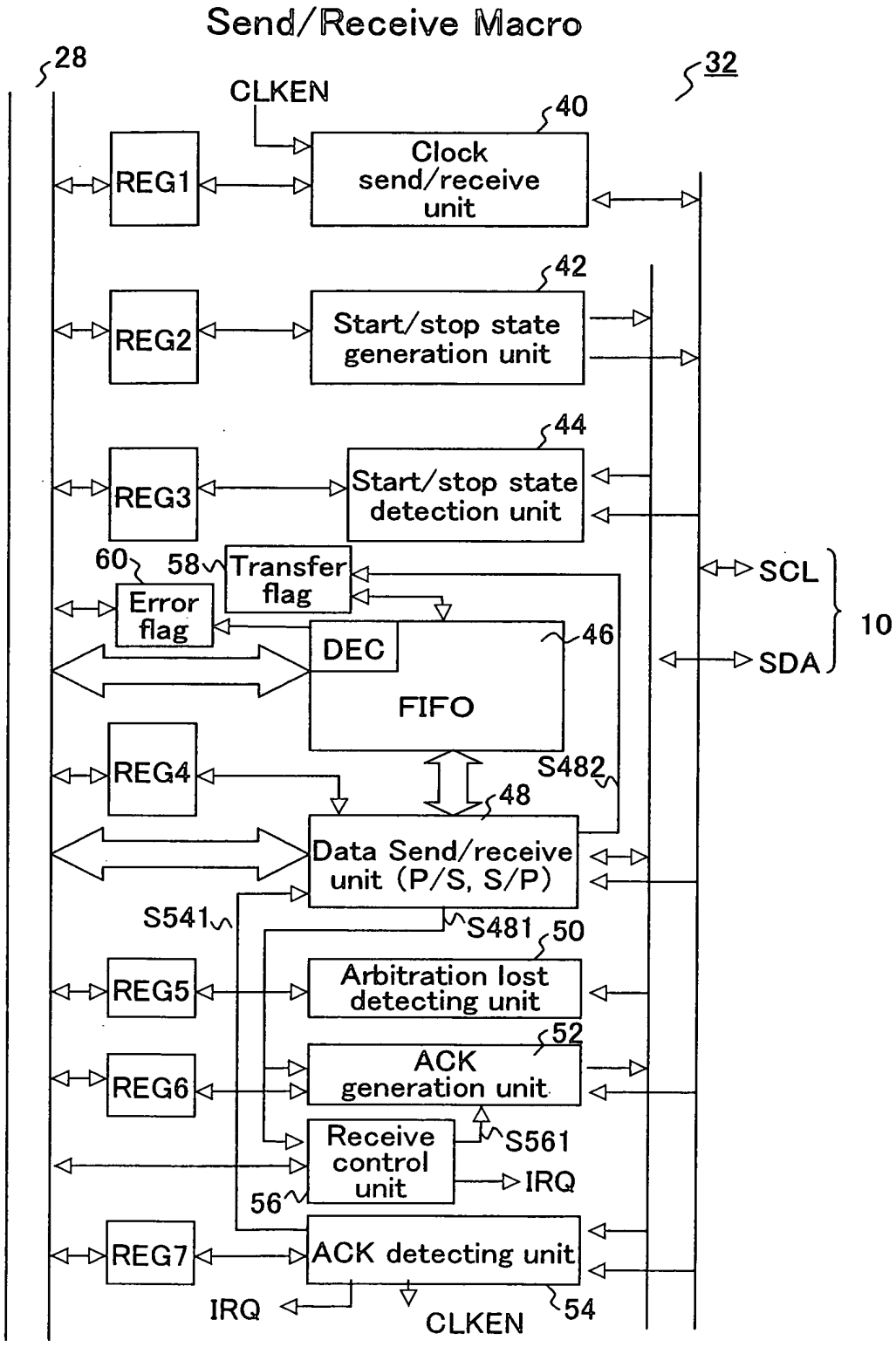

Send/Receive Macro
28
32
CLKEN
40
Clock send/receive unit
REG1
42
Start/stop state generation unit
REG2
44
Start/stop state detection unit
REG3
60
58
Transfer flag
Error flag
DEC
FIFO
46
SCL
SDA
10
REG4
S482
48
Data Send/receive unit (P/S, S/P)
S541
S481
50
Arbitration lost detecting unit
REG5
52
ACK generation unit
REG6
Receive control unit
S561
IRQ
56
REG7
ACK detecting unit
IRQ
CLKEN
54

FIG. 4

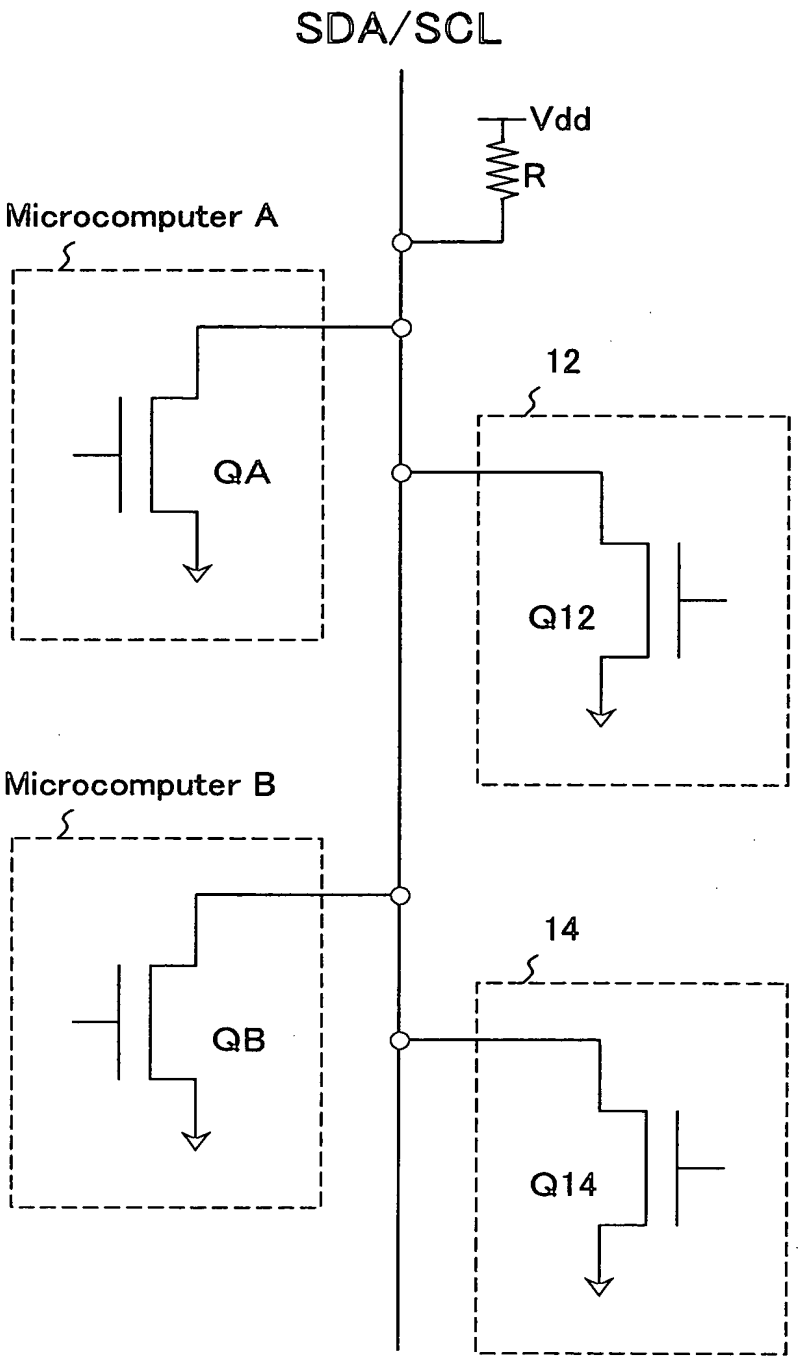

SDA/SCL
Vdd
R
Microcomputer A
12
QA
Q12
Microcomputer B
14
QB
Q14

FIG. 5

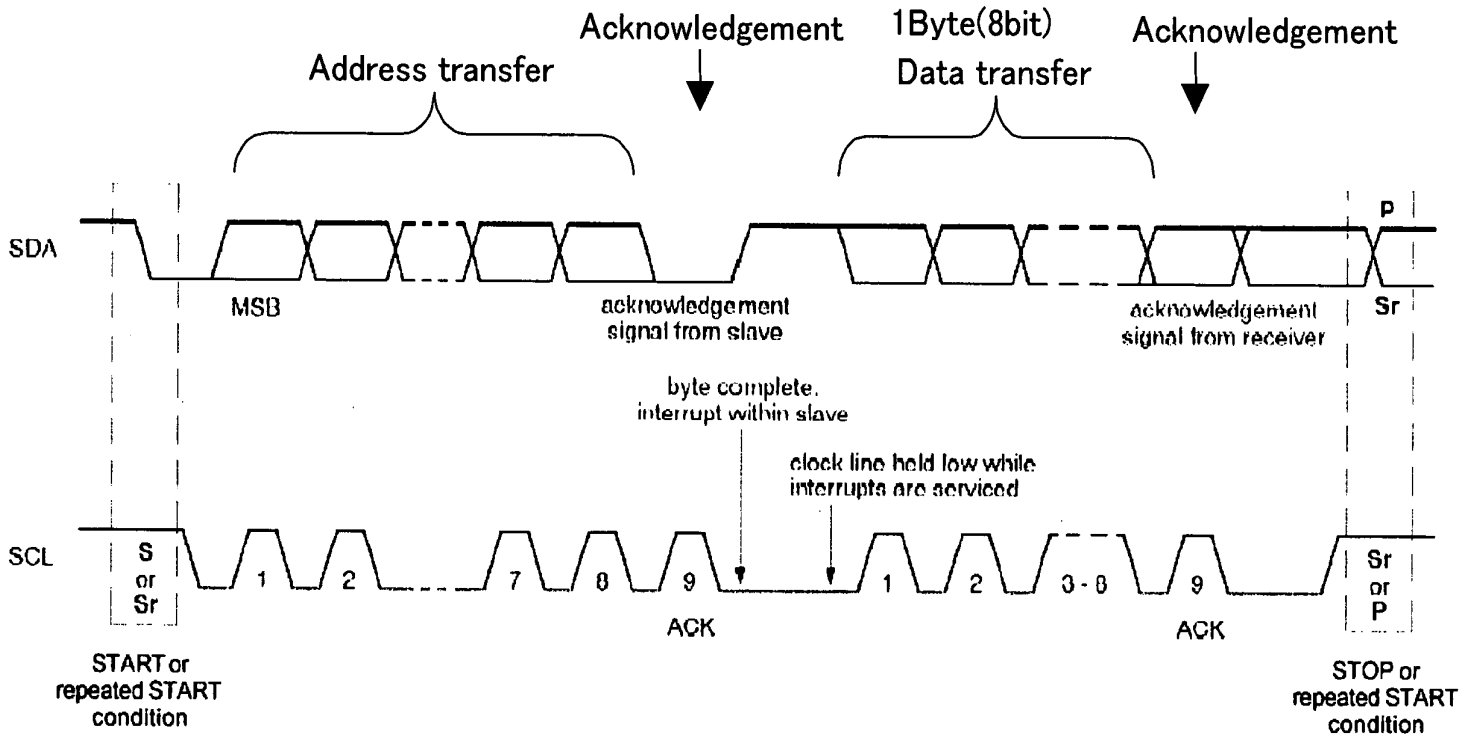

Acknowledgement
1Byte(8bit)
Acknowledgement
Address transfer
Data transfer
SDA
P
MSB
acknowledgement signal from slave
acknowledgement signal from receiver
Sr
byte complete, interrupt within slave
clock line held low while interrupts are serviced
SCL
S or Sr
1
2
7
8
9
1
2
3 - 8
9
Sr or P
ACK
ACK
START or repeated START condition
STOP or repeated START condition

FIG. 6

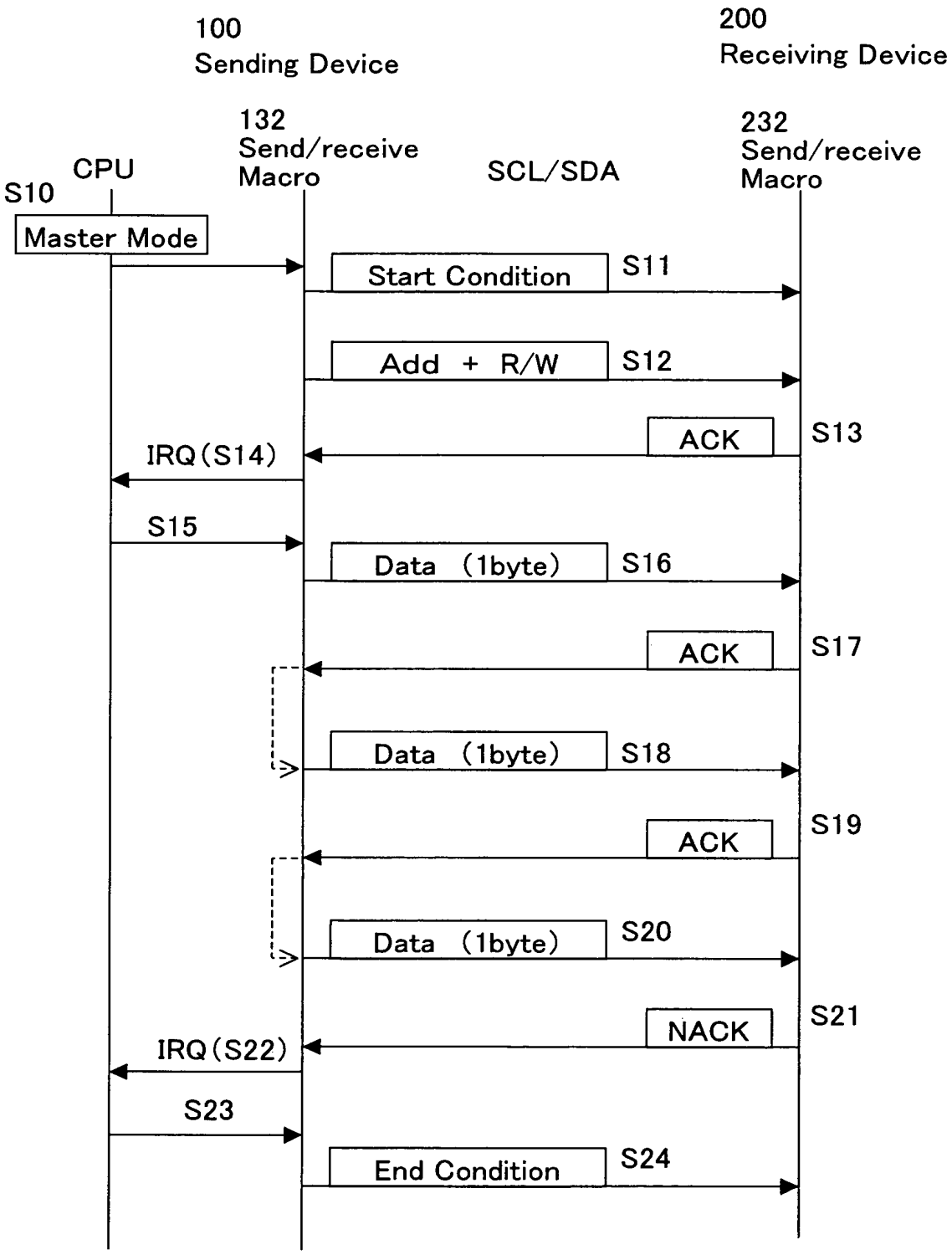

100
Sending Device
200
Receiving Device
132
Send/receive
Macro
232
Send/receive
Macro
CPU
SCL/SDA
S10
Master Mode
Start Condition
S11
Add + R/W
S12
ACK
S13
IRQ(S14)
S15
Data (1byte)
S16
ACK
S17
Data (1byte)
S18
ACK
S19
Data (1byte)
S20
NACK
S21
IRQ(S22)
S23
End Condition
S24

FIG. 7A

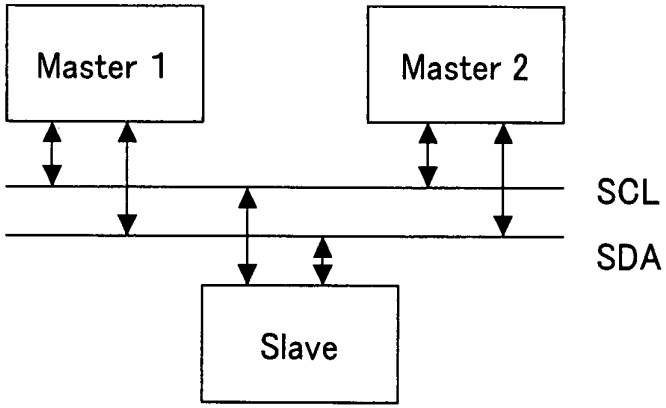

Master 1
Master 2
SCL
SDA
Slave

FIG. 7B

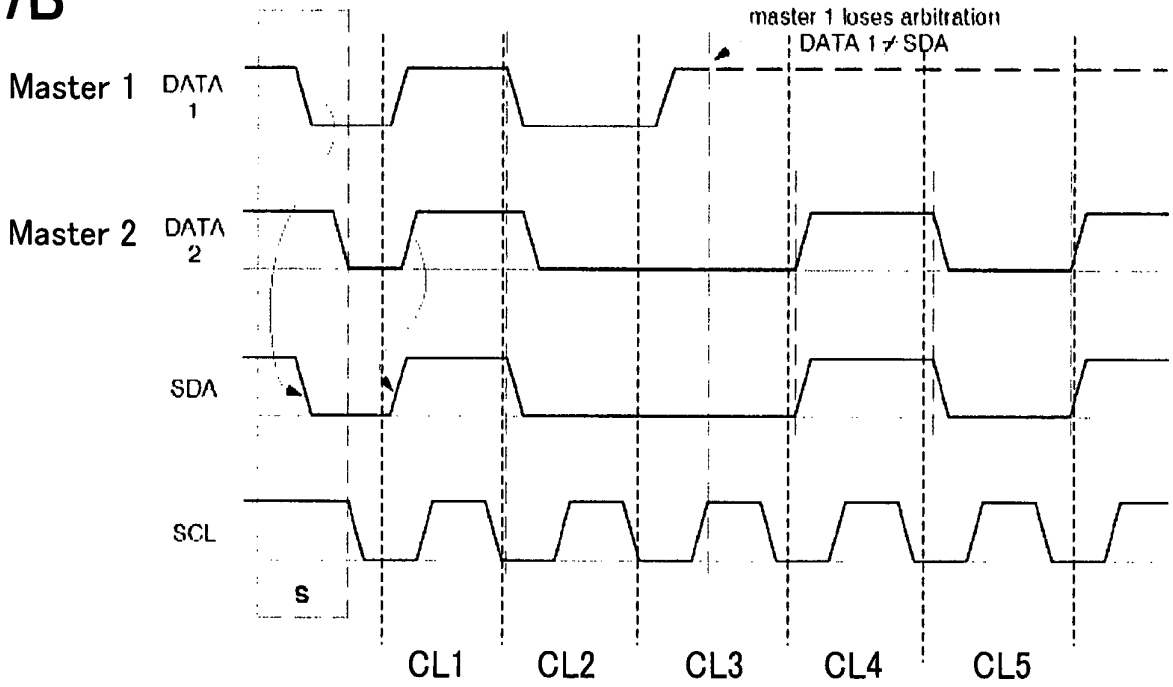

master 1 loses arbitration
DATA 1 ≠ SDA
Master 1
DATA 1
Master 2
DATA 2
SDA
SCL
S
CL1
CL2
CL3
CL4
CL5

FIG. 8

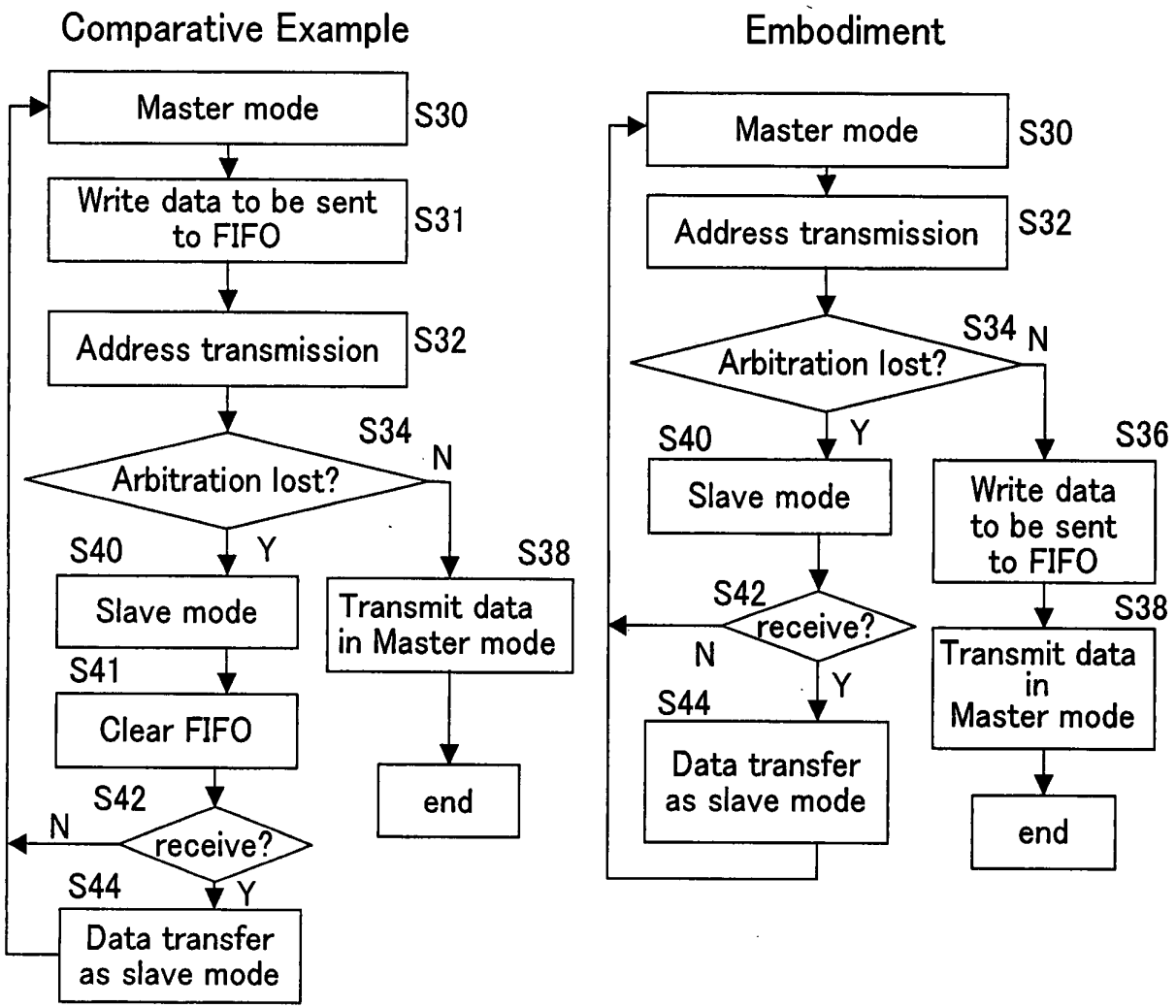

Comparative Example
Master mode
S30
Write data to be sent to FIFO
S31
Address transmission
S32
S34
Arbitration lost?
N
Y
S40
Slave mode
S41
Clear FIFO
S42
receive?
N
Y
S44
Data transfer as slave mode
S38
Transmit data in Master mode
end
Embodiment
Master mode
S30
Address transmission
S32
S34
Arbitration lost?
N
Y
S40
Slave mode
S42
receive?
N
Y
S44
Data transfer as slave mode
S36
Write data to be sent to FIFO
S38
Transmit data in Master mode
end

FIG. 9

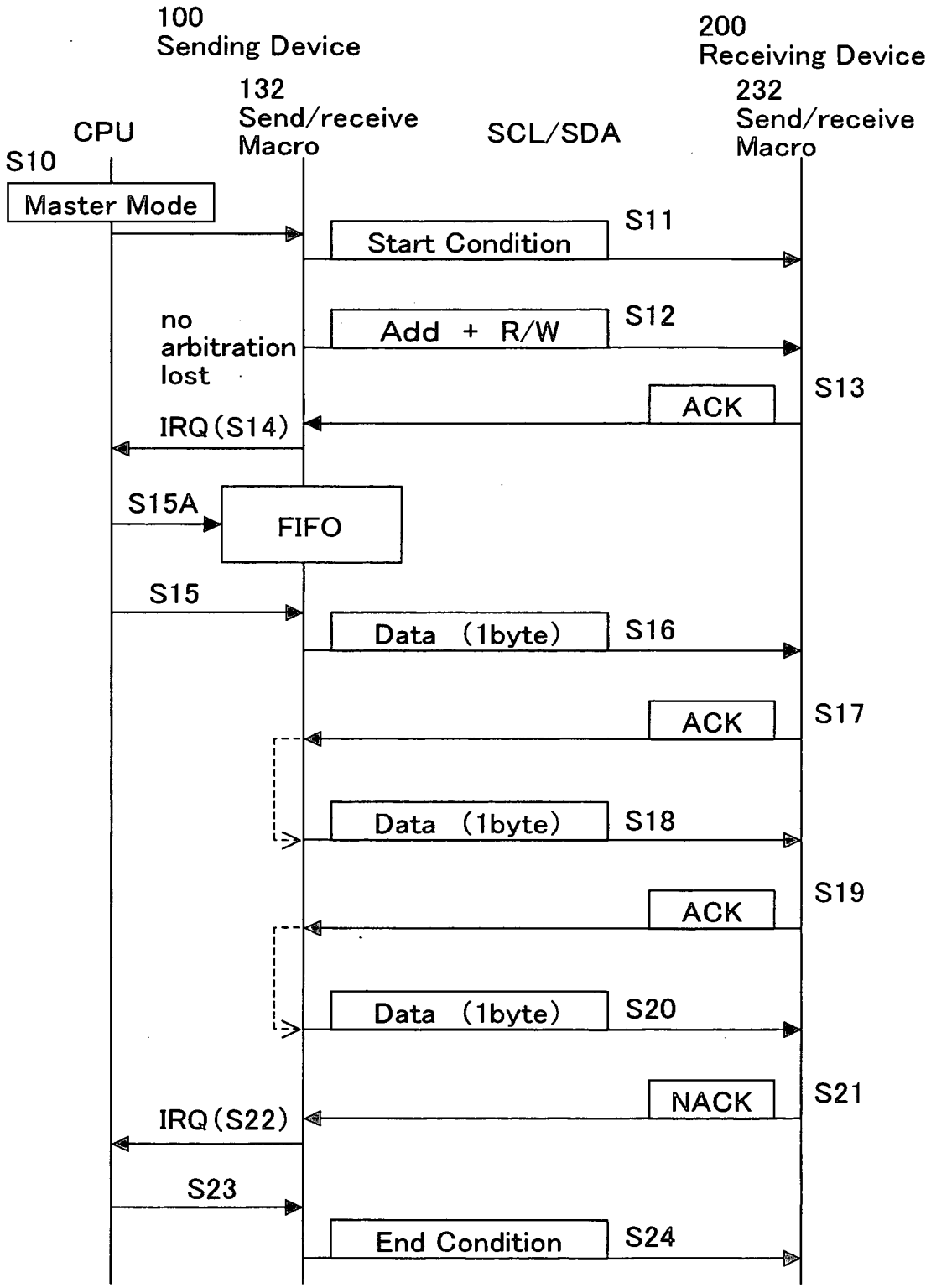

100
Sending Device
132
Send/receive
Macro
CPU
SCL/SDA
200
Receiving Device
232
Send/receive
Macro
S10
Master Mode
Start Condition
S11
no
arbitration
lost
Add + R/W
S12
ACK
S13
IRQ(S14)
S15A
FIFO
S15
Data (1byte)
S16
ACK
S17
Data (1byte)
S18
ACK
S19
Data (1byte)
S20
NACK
S21
IRQ(S22)
S23
End Condition
S24

FIG. 10

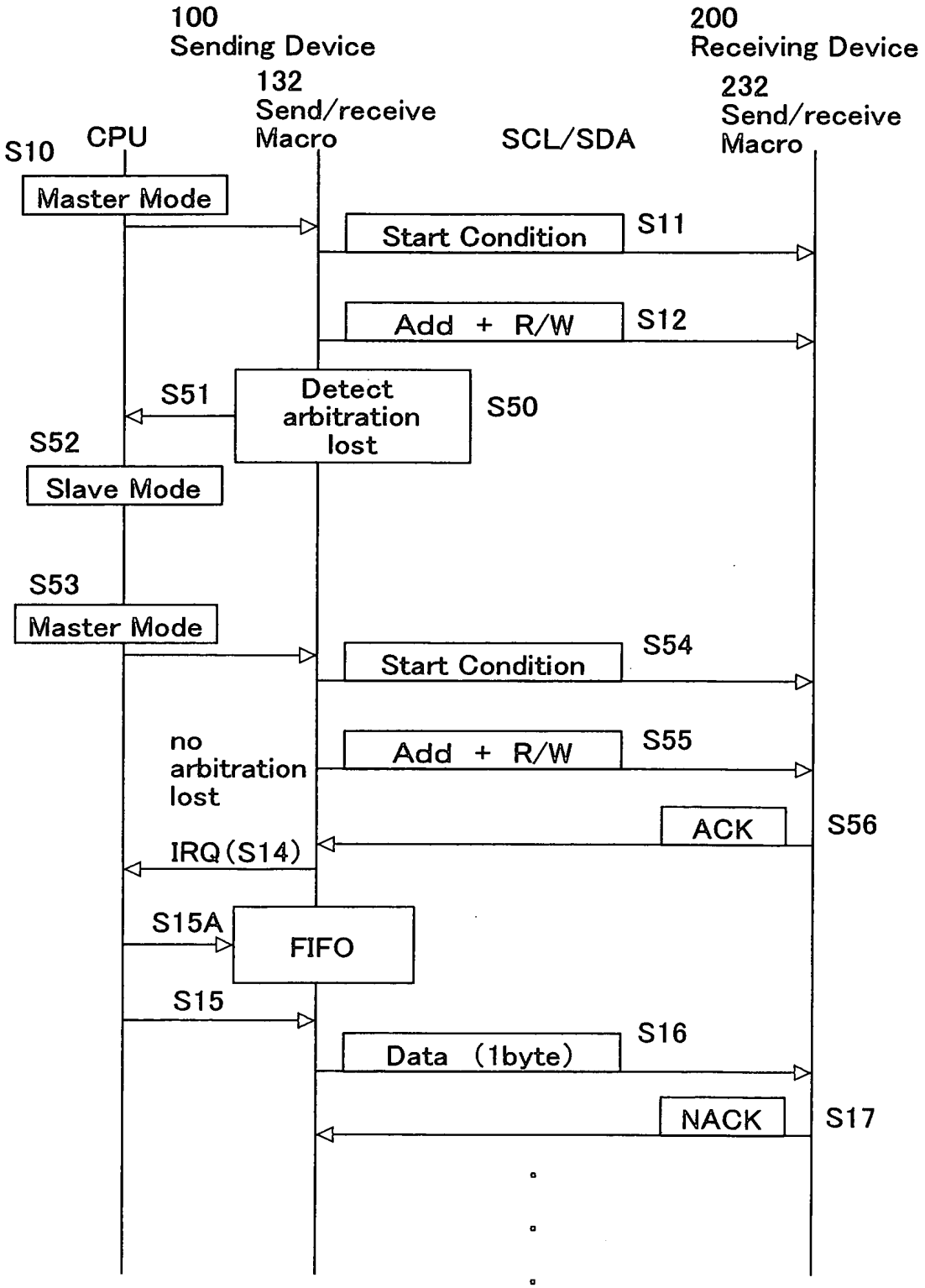

100
Sending Device
132
Send/receive
Macro
200
Receiving Device
232
Send/receive
Macro
S10
CPU
SCL/SDA
Master Mode
Start Condition
S11
Add + R/W
S12
S51
Detect
arbitration
lost
S50
S52
Slave Mode
S53
Master Mode
Start Condition
S54
no
arbitration
lost
Add + R/W
S55
ACK
S56
IRQ(S14)
S15A
FIFO
S15
Data (1byte)
S16
NACK
S17

FIG. 11

Third Embodiment

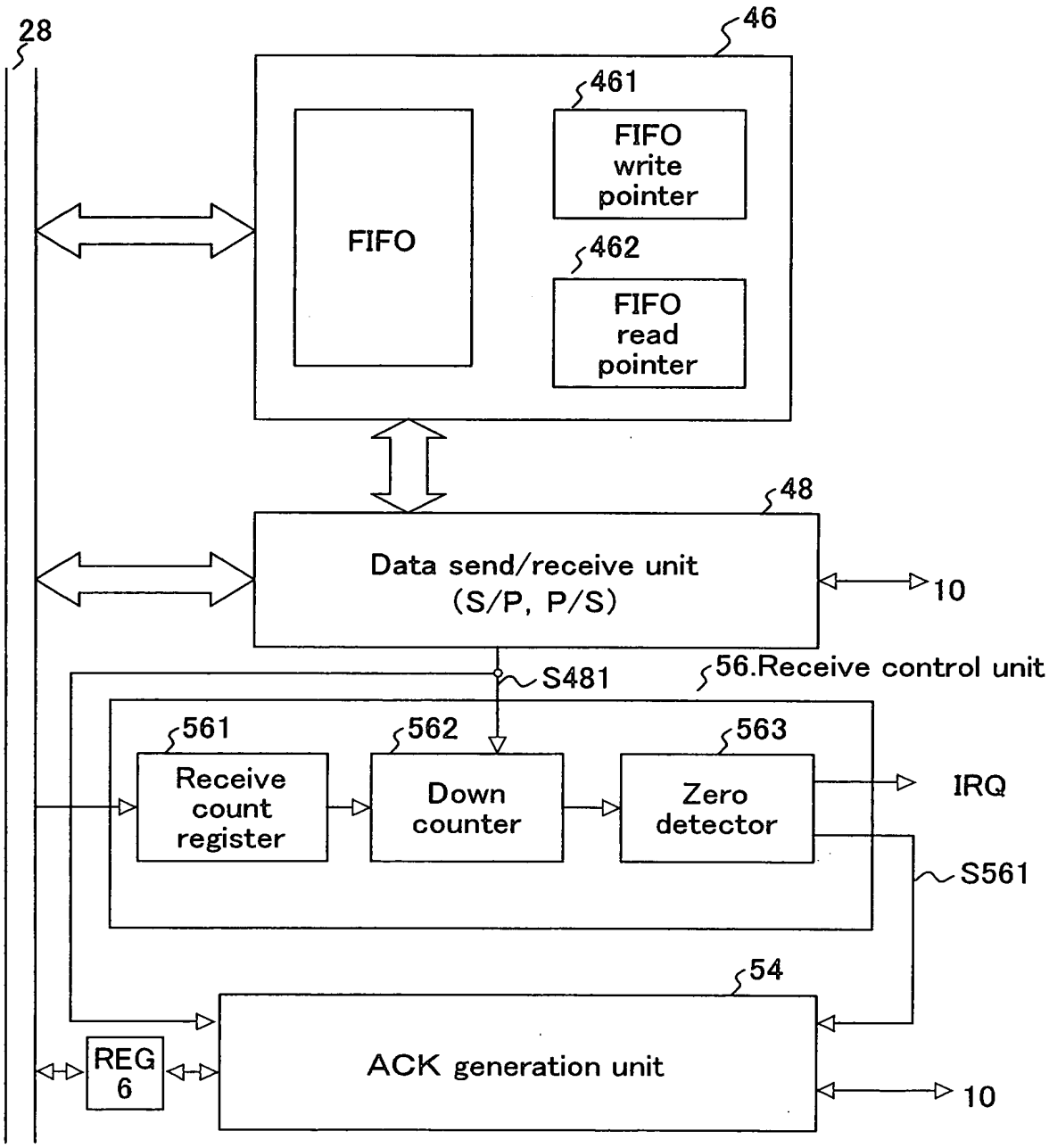
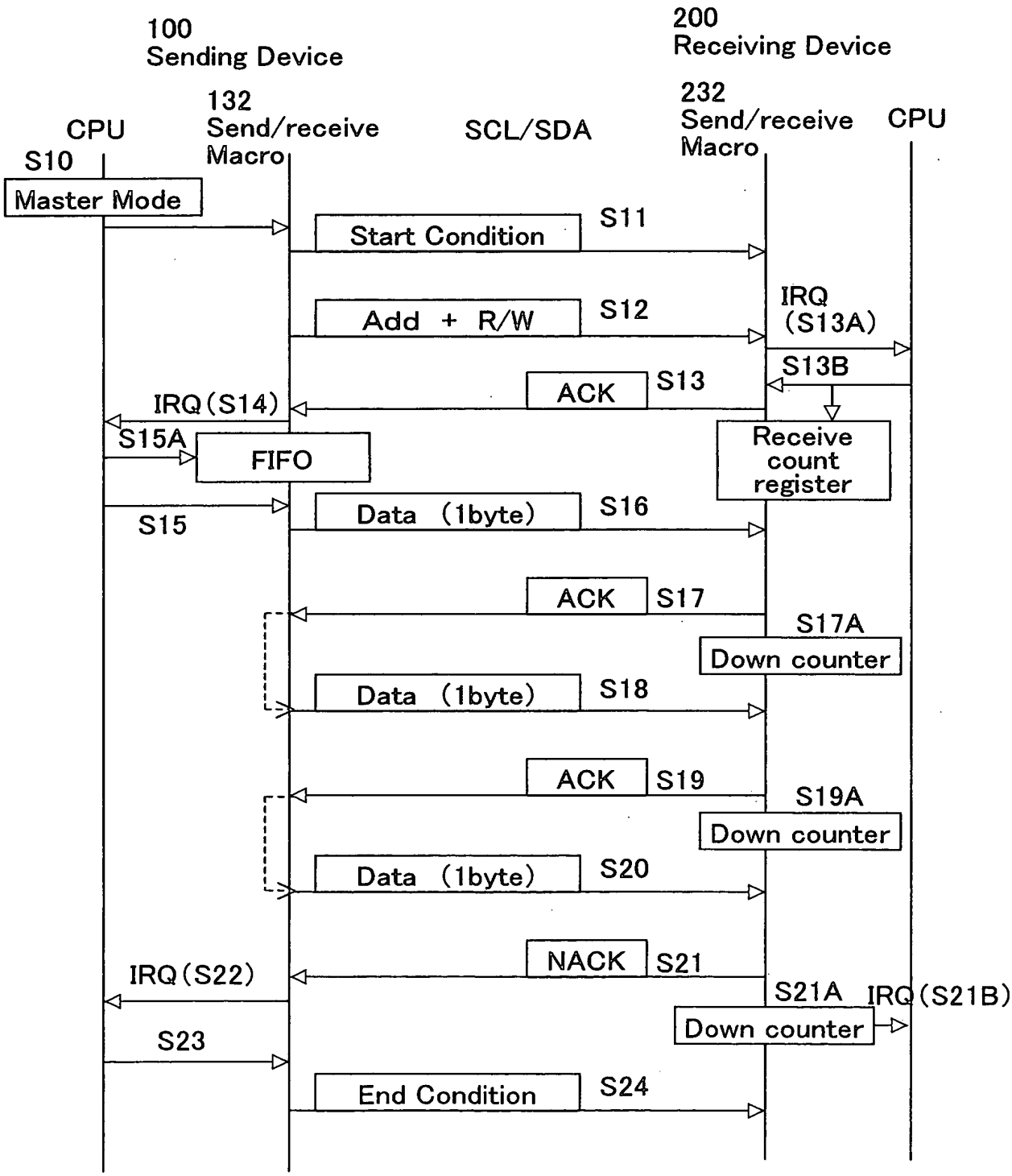


FIG. 12


100
Sending Device
200
Receiving Device
CPU
132
Send/receive
Macro
SCL/SDA
232
Send/receive
Macro
CPU
S10
Master Mode
Start Condition
S11
Add + R/W
S12
IRQ
(S13A)
S13B
ACK
S13
IRQ(S14)
S15A
FIFO
Receive
count
register
S15
Data (1byte)
S16
ACK
S17
S17A
Down counter
Data (1byte)
S18
ACK
S19
S19A
Down counter
Data (1byte)
S20
NACK
S21
IRQ(S22)
S21A
IRQ(S21B)
Down counter
S23
End Condition
S24